	ATTY. DOCKET NO. 1875.3750001/RES/GSB	APPLICATION NO. To Be Assigned 10, 812, 97
FORM PTO-1449	FIRST NAMED INVENTOR Minsheng WANG	
INFORMATION DISCLOSURE STATEMENT	FILING DATE Herewith (March 31, 2004)	ART UNIT To Be Assigned 2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
KN	AA1	US-5,305,004	04/1994	Fattaruso, John W.	341	120	
KN	AB1	US-5,404,142	04/1995	Adams et al.	341	144	
KN	AC1	US-6,124,813	09/2000	Robertson et al.	341	143	
KN	AD1	US-6,570,521	05/2003	Schofield, William G. J.	341	144	
KN	AE1	US-6,577,261	06/2003	Brooks et al.	341	144	
KN	AF1	US-6,614,377	09/2003	Adams et al.	341	144	
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

KN	AR	1	Adams, R. et al., "A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," *IEEE Journal of Solid-State Circuits* 33:12:1879-1886 (December 1998)
KN	AS	1	Annovazzi, M. et al., "A Low-Power 98-dB Multibit Audio DAC in a Standard 3.3-V 0.35-μm CMOS Technology," *IEEE Journal of Solid-State Circuits* 37:7:825-834 (July 2002)
KN	AT	1	Baird, R. and Fiez, T., "Improved ΔΣ DAC Linearity Using Data Weighted Averaging," *IEEE*, pp. 13-16 (1995)

EXAMINER Nguyenlhee	DATE CONSIDERED 07/15/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449	ATTY. DOCKET NO. 1875.3750001/RES/GSB	APPLICATION NO. To Be Assigned *10/812,975*
	FIRST NAMED INVENTOR Minsheng WANG	
INFORMATION DISCLOSURE STATEMENT	FILING DATE Herewith (March 31, 2004)	ART UNIT To Be Assigned *2819*

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

KN	AR	2	Chen, F. and Leung, B., "Some Observations on Tone Behavior in Data Weighted Averaging," *Proceedings of the IEEE 1998 International Symposium on Circuits and System*, I-500 through I-503 (May 31 - June 3, 1998)
KN	AS	2	Chen, K. and Kuo, T., "An Improved Technique for Reducing Baseband Tones in Sigma-Delta Modulators Employing Data Weighted Averaging Algorithm Without Adding Dither," *IEEE Transactions on Circuits and Systems- II: Analog and Digital Signal Processing* 46:1:63-68 (January 1999)
KN	AT	2	Fishov, A. et al., "Segmented Mismatch-Shaping D/A Conversion," *IEEE*, pp. IV-679 through IV-682 (2002)

EXAMINER *Nguyen Khai*	DATE CONSIDERED *07/15/04*

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	FIRST NAMED INVENTOR Minsheng WANG	
INFORMATION DISCLOSURE STATEMENT	FILING DATE Herewith (March 31, 2004)	ART UNIT To Be Assigned 2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

KN	AR	3	Folgeman, E. and Galton, I., "A Digital Common-Mode Rejection Technique for Differential Analog-to-Digital Conversion," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing* 48:3:255-271 (March 2001)
KN	AS	3	Galton, I., "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," *IEEE Transactions on Circuits and System-II: Analog and Digital Signal Processing* 44:10:808-817 (October 1997)
KN	AT	3	Grilo, J. *et al.*, "A 12-mW ADC Delta-Sigma Modulator With 80dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," *IEEE Journal of Solid-State Circuits* 37:3:271-278 (March 2002)

EXAMINER Nguyenkha	DATE CONSIDERED 07/15/04

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FORM PTO-1449	ATTY. DOCKET NO. 1875.3750001/RES/GSB	APPLICATION NO. To Be Assigned 10/812,975
	FIRST NAMED INVENTOR Minsheng WANG	
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U.S. PATENT DOCUMENTS

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	AA4						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

KN	AR	4	Jensen, H. and Galton, I., "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis," *IEEE Transactions on Circuits and Systems- II: Analog and Digital Signal Processing*, 45:1:13-27 (January 1998)
KN	AS	4	Kwan, T. *et al.*, "A Stereo Multibit $\Sigma\Delta$ DAC with Asynchronous Master-Clock Interface," *IEEE Journal of Solid-State Circuits* 31:12:1881-1887 (December 1996)
KN	AT	4	Norsworthy, S.R. *et al.*, eds., "Practical Measures for Preventing Idle Tones" in *Delta-Sigma Data Converters: Theory, Design and Simulation, IEEE Press*, pp. 185-186 (1997)

EXAMINER Nguyenkhal	DATE CONSIDERED 07/15/04

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FORM PTO-1449				FIRST NAMED INVENTOR Minsheng WANG				
INFORMATION DISCLOSURE STATEMENT				FILING DATE Herewith (March 31, 2004)		ART UNIT To Be Assigned 2819		

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

KN	AR	5	Radke, R. et al., "A Spurious-Free Delta-Sigma DAC Using Rotated Data Weighted Averaging," *Proceedings of the IEEE 1999 Custom Integrated Circuits Conference*, pp. 125-128 (May 16 - 19, 1999)
KN	AS	5	Radke, R. et al., "A 14-Bit Current-Mode $\Sigma\Delta$ DAC Based Upon Rotated Data Weighted Averaging," *IEEE Journal of Solid-State Circuits* 35:8:1074-1084 (August 2000)
KN	AT	5	Vadipour, M., "Techniques for Preventing Tonal Behavior of Data Weighted Averaging Algorithm in Σ-Δ Modulators," *IEEE Transactions on Circuits and Systems- II: Analog and Digital Signal Processing, Transactions on Circuits and Systems- II: Analog and Digital Signal Processing* 47:11:1137-1144 (November 2000)

EXAMINER Nguyenkhai	DATE CONSIDERED 07/15/04

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INFORMATION DISCLOSURE STATEMENT	**FILING DATE** Herewith (March 31, 2004)	**ART UNIT** To Be Assigned 2819

U.S. PATENT DOCUMENTS

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	AA6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

χN	AR	6	Welz, J. et al., "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing* 48:11:1014-1027 (November 2001)
kN	AS	6	Welz, J. and Galton, I., "A Necessary and Sufficient Condition for Mismatch Shaping in Multi-bit DACS," *IEEE*, pp. I-105 through 108 (2002)
$\mathcal{U}N$	AT	6	Yasuda, A. et al., "A Third-Order Δ-Σ Modulator Using Second-Order Noise Shaping Dynamic Element Matching," *IEEE Journal of Solid-State Circuits* 33:12:1879-1886 (December 1998)

EXAMINER Nguyen Khao	DATE CONSIDERED 07/15/04

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FORM PTO-1449			**FIRST NAMED INVENTOR** Minsheng WANG		
INFORMATION DISCLOSURE STATEMENT			**FILING DATE** Herewith (March 31, 2004)		**ART UNIT** To Be Assigned 2819

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	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

KN	AR	7	Zelniker, G. and Taylor, F., "Chapter 7: Multirate Signal Processing" in *Advance Digital Signal Processing: Theory and Applications*, Marcel Dekker, Inc., New York, NY, pp. 343-361 (1994).
	AS	7	
	AT	7	

EXAMINER *Nguyenkhap*	DATE CONSIDERED 07/15/04

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